Lecture 3

Rules:

$1+1=1$ $\quad$ $1\cdot 1=1$

$0+0=0$ $\quad$ $1\cdot 0=0$

$0+1=1$ $\quad$ $0\cdot 0=0$

$a+a=a$ $\quad$ $a\cdot 1=a$ $\quad$ $a+1=1$

$a\cdot a=a$ $\quad$ $a\cdot 0=a$ $\quad$ $a+0=a.$

$ab+ac=a(b+c)$ (Distributive)

Simplification

$ab+ab' = a(b+b') = a$

$ab'+a'b = a\oplus b$

$ab+a'b' = (a\oplus b)'$

A	B	Q
0	0	0+0 = 0
0	1	0+1 = 1
1	0	1+0 = 1
1	1	0+0 = 0

} XOR.

$a'bc_i + ab'c_i + abc_i' + abc_i$

$= a'bc_i + ab'c_i + ab + abc_i$

$= a'bc_i + ac_i + ab + abc_i$

$a'bc_i + ab'c_i + abc_i' + abc_i$

$+ abc_i + abc_i$

$bc_i + ac_i + ab$

Full Adder

When we add in decimal, we add in places

```
 11
 373
+198
----
 571
```

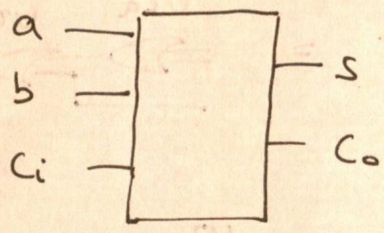
At any given place, we have two inputs (e.g. 7 and 9) and possibly a carry.

```
  1
 373
+198
----
 571
```

=> 3 inputs, call them a, b, c_i
(1st #, 2nd #, "carry in")

We get two outputs: the sum number and a possible carry (s, c_o).

```
(1)1
 373
+198
----
 5(7)1
```



"Full adder" for only adding two bits and a carry.

e.g. $(a=1) + (b=0) + (c_i=1) \Rightarrow (s=0)$, with $(c_o=1)$.

"plus", not "OR"

```
  1  carry
  1  a
+ 0  b
----
 10
```

Truth Table

a	b	c_i	s	c_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equations

$$s = a'b'c_i + a'bc_i' + ab'c_i' + abc_i$$

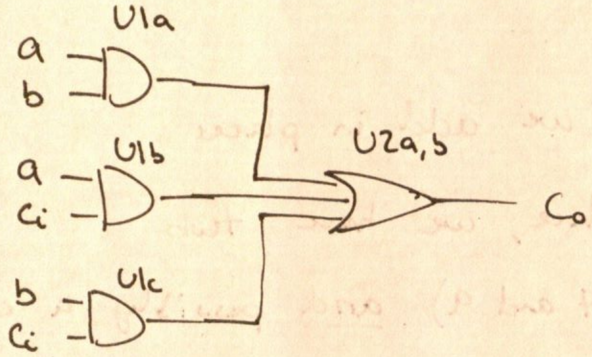
$$= a'(b \oplus c_i) + a(b \oplus c_i)'$$

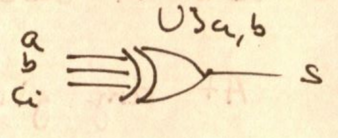
$$\boxed{s = a \oplus b \oplus c_i}$$

$$c_o = a'bc_i + ab'c_i + abc_i' + abc_i + abc_i + abc_i \quad (\Leftarrow \text{extras!})$$

$$\boxed{c_o = bc_i + ac_i + ab}$$

Not the only way to simplify!



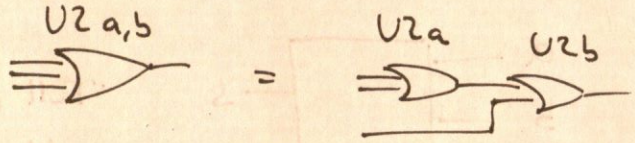


74 HC 08 : Quad 2-input AND gate. (1) (use 3)

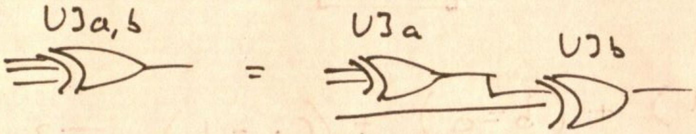
74 HC 32 : Quad 2-input OR gate (1) (use 2)

74 HC 86 : Quad 2-input XOR gate (1) (use 2)

Note:



And



Parity Bit Generator

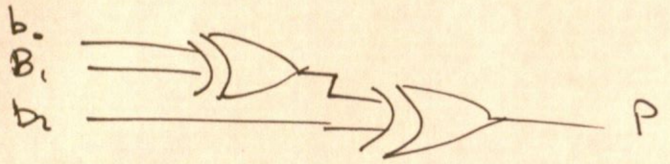
"Even Parity"

b_2 b_1 b_0	P
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1

$$P = b_2' b_1' b_0 + b_2' b_1 b_0' + b_2 b_1' b_0' + b_2 b_1 b_0$$

$$P = b_2' \oplus (b_1 \oplus b_0) + b_2 (b_1 \oplus b_0)'$$

$$P = b_2' \oplus b_1 \oplus b_0.$$



2.59

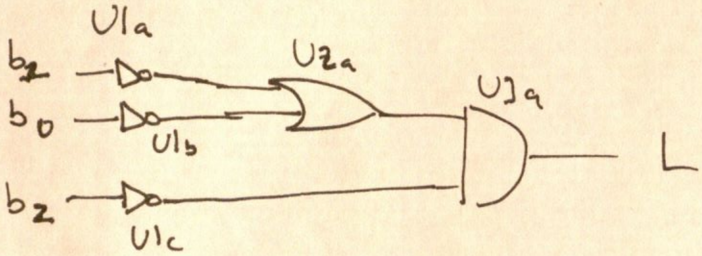
b_2 b_1 b_0	L
0 0 0	1
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	0
1 0 1	0
1 1 0	0
1 1 1	0

$$L = \underbrace{b_2' b_1' b_0' + b_2' b_1' b_0} + b_2' b_1 b_0'$$

$$L = b_2' b_1' b_0' + b_2' b_1' b_0 + b_2' b_1 b_0' + \boxed{b_2' b_1' b_0'}$$

$$L = b_2' b_1' + b_2' b_0'$$

$$L = b_2' (b_1' + b_0')$$



74 HC 04 Hex Inverter.

74 HC 08 Quad 2-input AND gate

74 HC 32 Quad 2-input OR gate.